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RMI STANDARDIZES ON AXIOM'S MPSIM FOR FUNCTIONAL VERIFICAITON

MILPITAS, Calif. May 17, 2005 — AXIOM Design Automation today announced that RMI (Raza Microelectronics, Inc), an innovative leader in silicon solutions designed to transform the Information Infrastructure, has standardized on MPSim™ for it's functional verification environment. RMI is using MPSim's native Compiled TestBench (CTB) and assertion technology to significantly speed up its IC verification process. MPSim is the only simulation product offering native integrated testbench, assertion based verification, coverage and debugging capabilities that leverages multi-CPU hardware to deliver up to 6x faster verification performance.

"We are now using MPSim as the default production simulator and have successfully taped out a 40M gate design using this product," said Rajat Roy, Vice President Product Development and General Manager, RMI Access and Processor Solutions. "MPSim's integrated OpenVera® testbench, SystemVerilog assertion and robust debugging capabilities have provided us with an immediate improvement in verification productivity."

"Customers achieve two levels of performance and productivity gain using MPSim." said Badru Agarwala, President and CEO of AXIOM. "The first level is achieved by using an integrated simulation environment that includes Verilog simulation, native Compiled TestBench (CTB) and SystemVerilog assertions. The second level of performance gain that is unique to MPSim is achieved by utilizing patent pending multi-CPU technology delivering up to 3x additional performance on 4 CPU hardware. MPSim has been architected such that its performance scales with the number of CPU's available on the hardware."

MPSim offers a compelling solution for creating a comprehensive testbench environment by providing full support for advanced verification languages including OpenVera and SystemVerilog as well as offering the highest performance commercially available simulator. CTB leverages core formal verification technology developed by AXIOM to deliver a robust and powerful constraint solver that simplifies the task of generating complex testbenchs. This ability to generate additional corner case scenarios, coupled with multi-CPU technology that can generate 6x more vectors, enables verification teams to identify design bugs missed by other solutions.

Availability

MPSim is available immediately. For more information on MPSim, please visit the AXIOM website at http://www.axiom-da.com .

About AXIOM

Originally founded as @HDL in 1999, AXIOM has been a pioneer in developing functional verification products. The company's mission has always been to accelerate the verification flow and to increase the overall productivity of verification engineers. The introduction of the MPSim multi-CPU simulator provides a quantum leap in verification performance to the industry and enables AXIOM to offer a complete solution to its customers.

AXIOM's integrated verification environment combines the fastest simulator in the industry with advanced testbench automation, assertion based verification, debugging and coverage analysis to ensure that your most complex designs are fully verified in the least amount of time. AXIOM supports commercially available hardware and industry standard languages including SystemVerilog, Verilog, OpenVera and PSL to ensure continuity with your existing verification methodology while offering a clear path to immediate productivity improvement.

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